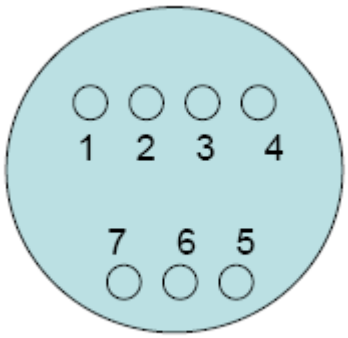
1 Pin arrangement:

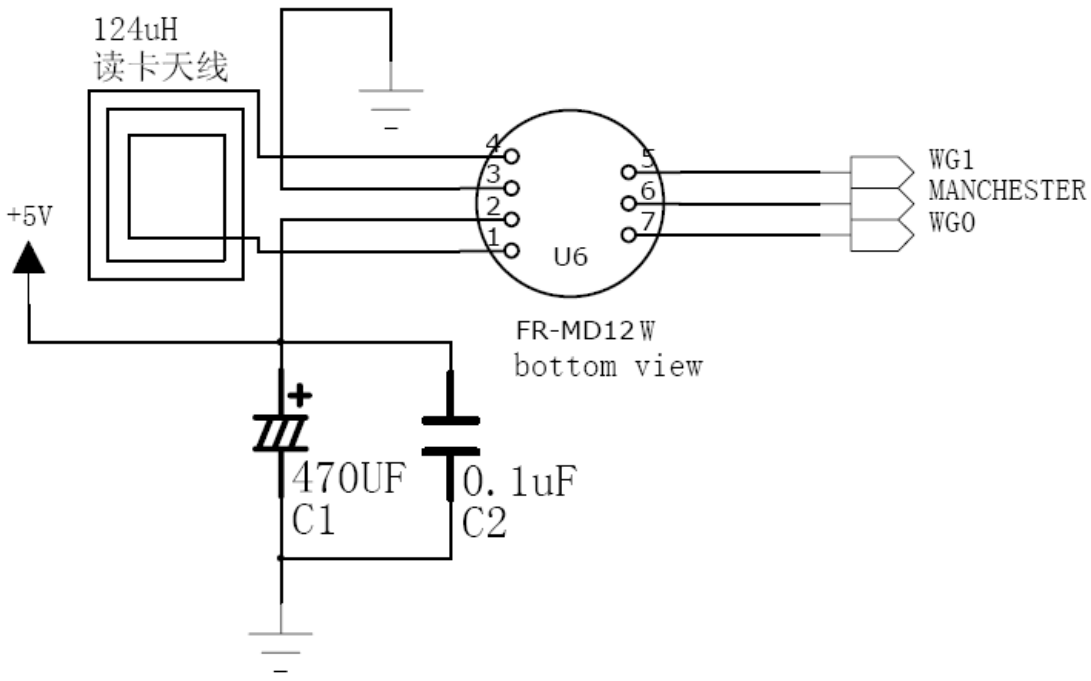



Bottom view

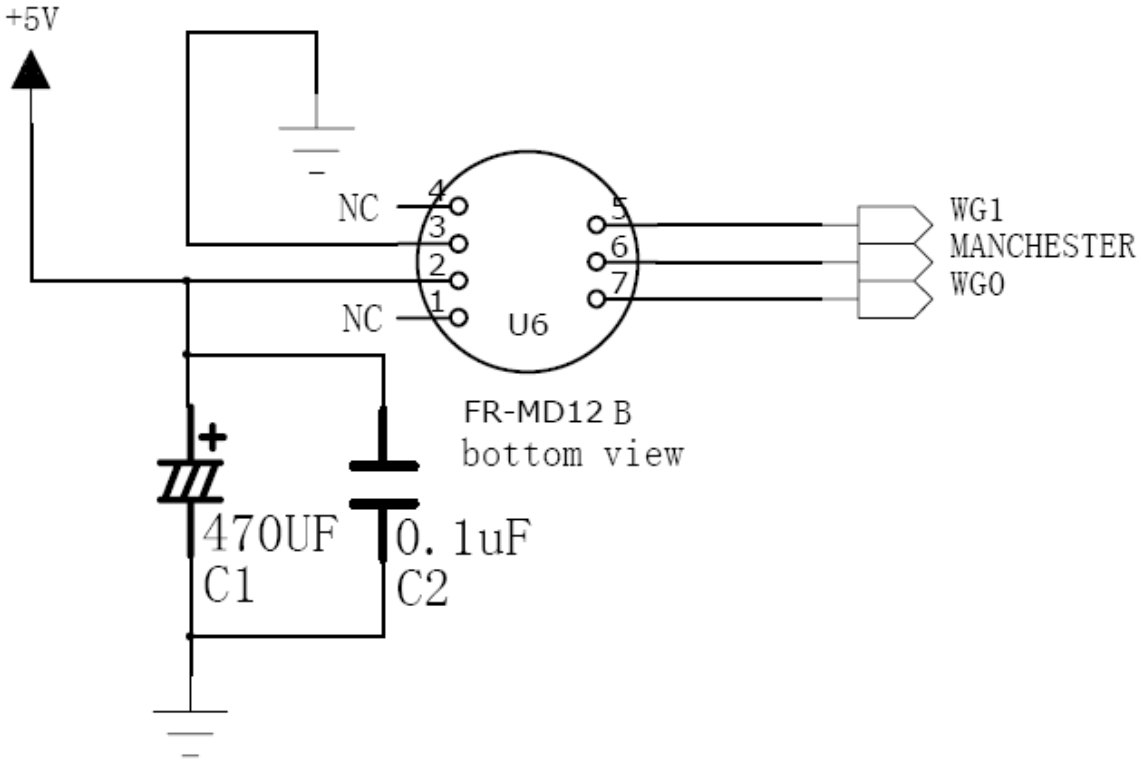
2 Pin description

| **PIN NUMBER** | **FUNCTION FR-MD12B** | **FUNCTION FR-MD12W** |
|---|---|---|
| 1 | NC | ANT1 124uH |
| 2 | Power Vdd | Power Vdd |
| 3 | Common Vss | Common Vss |
| 4 | NC | ANT2 124uH |
| 5 | Data One (WG1) | Data One (WG1) |
| 6 | MManchester code out | Manchester code out |
| 7 | Data Zero (WG0) | Data Zero (WG0) |

3 FR-MD12W Type application



FR-MD12B Type Application




4 DC characteristic

| | |
|---|---|
| Power Supply Type | Linear Type recommended |
| Operating Voltage Range | 3.0 -5.5VDC |
| Maximum Input Current | <50mA (Average at 5V) |
| RF Modulation | 26-Bit Wiegand -ASK |
| Card Read Distance: | Min 40- 60mm FOR FR-MD12B<br>Min 80- 90mm FOR FR-MD12W<br>Depending on transponder and antenna. |
| Operating Temp. Range: | -31 ℃ to63 ℃(-25 F to145 F) |
| Operating Humidity: | 0 to 95% (non condensing) |
| Dimensions: | 12mm Radius, 9.0mm Depth |

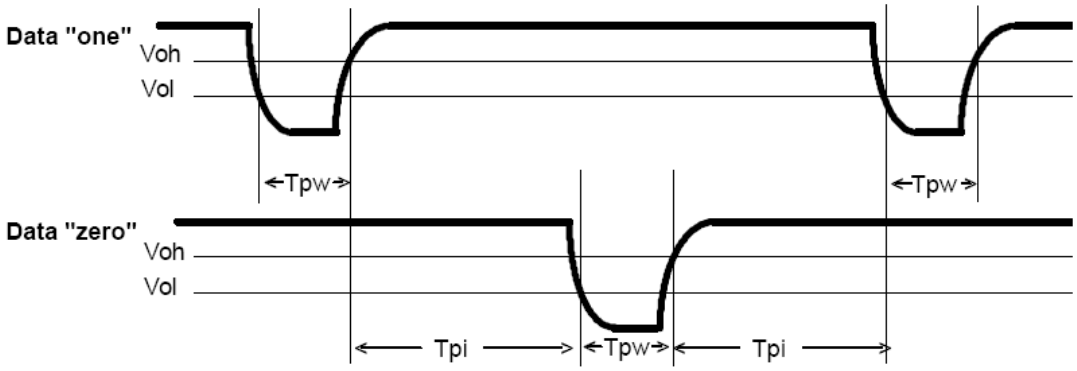
5 **Signal Levels**

The Data One and Data Zero provide logic signals between the reader and the panel.
The logic voltage levels are measured at the reader.
Both Data One and Data Zero have 1kΩ resistor in output series.
The logic voltage levels are defined as follows:

| Voltage Levels | Data Outputs (Data 1 and 0) | |
|---|---|---|
| | **Minimum** | **Maximum** |
| Voh | Power Supply - 0.7 | - V |
| Vol | - | 0.7 V |
| Ioh | 4.5 | 5.5 mA |
| Iol | -1.0 | -10 μA |

## 6 Data Pulses

The Data One and Data Zero signals are normally held at a logic high level until the reader is ready to send a data stream. The reader places asynchronous low going pulses on the appropriate data lines to transmit the data stream to the panel. The data pulses for the Data One and Data Zero shall not overlap or occur simultaneously. The following timing parameters shall be observed:




| SYMBOL | DESCRIPTION | MINIMUM | MAXIMUM |
|---|---|---|---|
| TPW | Pulse Width Time | 20us | 60us |
| TPI | Pulse Interval Time | 1500us | 2500us |

## 7 Data Format

The 26 bits of transmission from the reader to the panel consists of two parity bits and 24 code bits. The bits are transmitted in the order described. The first bit transmitted is the first parity bit, P1, it is even parity calculated over the first 12 code bits. The last bit transmitted is the second parity bit, P2, it is odd parity calculated over the last 12 code bits:

CODE FORMAT

| | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0 | 1 | 2 | 3 | 4 | 5 | 6 |
| P1 | C | C | C | C | C | C | C | C | C | C | C | C | C | C | C | C | C | C | C | C | C | C | C | C | P2 |

PARITY FORMAT

| | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0 | 1 | 2 | 3 | 4 | 5 | 6 |
| P1 | E | E | E | E | E | E | E | E | E | E | E | E | | | | | | | | | | | | | |
| | | | | | | | | | | | | | O | O | O | O | O | O | O | O | O | O | O | O | P2 |

| | |
|---|---|
| P1: | First, or even parity bit. |
| C: | Code bits. |
| P2: | Second, or odd parity bit. |
| E: | Bits for calculation of even parity. |
| O: | Bits for calculation of odd parity. |

Data format within the 24 code bit that includes the partitioning of the bit.
Most Significant Bit (MSB) is outputting first.
EM4002 contain 40 bits of data. The reader implement to least 24 bits, add the parity bits and ignore the rest of the Data.

8 All size of the module: