Application Note 404

Title: **EM4095 Application Note**

Product Family: **RFID**

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TABLE OF CONTENT

1 Introduction

This application note introduces the CMOS integrated transceiver circuit EM4095 for RFID applications working with transponders at a frequency of typically 125 kHz. The paper describes the interoperability with a read-only and a read/write transponder in specific examples.

The application note offers helpful design guidelines. Firstly, an technical overview on the EM4095 is given. Secondly, the designer obtains practical design tips. Designing a typical reader circuit setup is shown by an example in the 4th chapter. The following chapters explain the interoperability of the EM4095 with read-only and read/write transponders.

Finally, EM Microelectronic-Marin SA offers a plug-and-play schematic for a typical reader setup using the EM4095. The corresponding PCB source files will be directly available from the homepage http://www.emmicroelectronic.com.

EM4095 Advantages

- low cost of external components
- ensured operation in resonance
- bigger area of reliable AM modulation
- easier analyze and system design due to only two system variables
- precise sampling positioning
- simple to use
- low power consumption

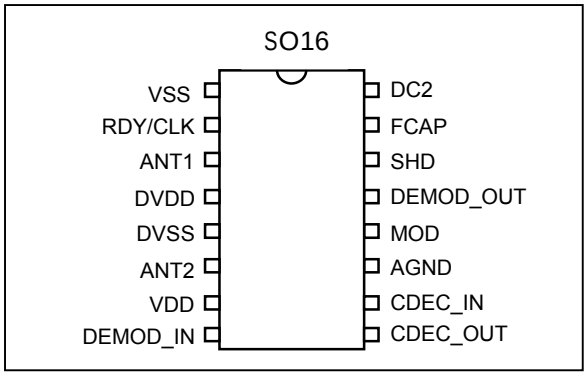


Figure 1: Pin Assignement

EM4095 features

- Integrated PLL system to achieve self adaptive carrier frequency to antenna resonant frequency
- No external quartz required
- 100 kHz to 150 kHz carrier frequency range
- Direct antenna driving using bridge drivers
- Data transmission by OOK (100% Amplitude Modulation) using bridge driver
- Data transmission by Amplitude Modulation with externally adjustable modulation index using single ended driver
- Multiple transponder protocol compatibility (e.g. EM400X, EM4050, EM4150, EM4070, EM4170, EM4069)
- Sleep mode 1µA
- USB compatible power supply range
- -40°C to +85°C temperature range
- Small outline plastic package SO16 or PSOP2 16

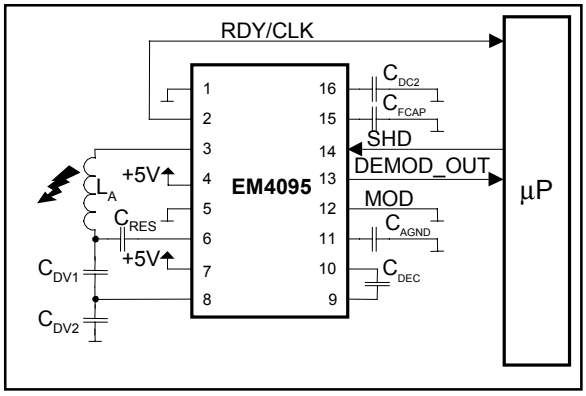


Figure 2: Typical operating configuration for read only mode

2 Operational Description

Technical background on how the EM4095 transceiver is operating is given in this chapter.

2.1 Resonant circuit parameters

In RFID system where RF frequency is defined by resonator there are three variables (resonant frequency of antenna, resonant frequency of transponder and RF driving frequency). In system using PLL there are only two variables, since the resonant frequency of the antenna and the RF driving frequency are the same.

The analysis shows that for a system having defined tolerances on antenna and transponder side the range where one demodulation chain (AM) with fixed sampling point can be used is much larger for PLL system. In fact taking in account technically achievable tolerances the resonator system using one sampling point is not feasible, two channels with 90° shifted sampling points are needed (AM/FM). This leads to more expensive system which is also more complex to operate.

A PLL system with one sampling point has also limitations for tolerance range of transponder and antenna. As a general rule can be notified; the higher the quality factors of the two resonant circuits are, the lower tolerances are acceptable (this is also true for a resonator system).

An RFID system with air transponder coils is normally not problematic. For transponders with a Q lower than 15, a tolerance of ±5 kHz on the antenna and transponder side is acceptable.

Transponders with ferrite core coils have usually higher quality factors (up to 40) and are therefore much more sensitive to tolerances.

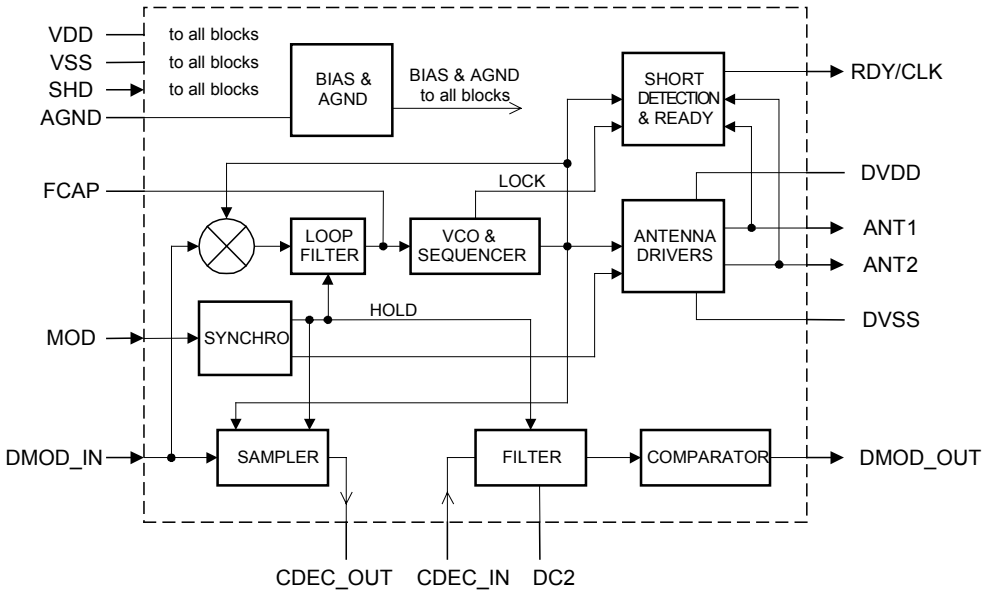
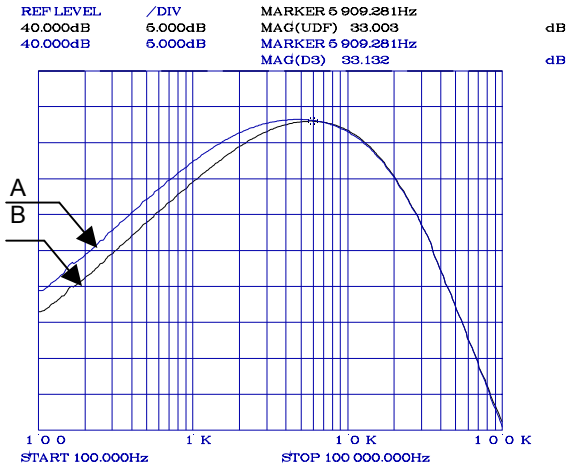


Figure 3: EM4095 Block Diagram

2.2 EM4095 architecture

The block diagram given in fig. 3 describes EM4095 architecture. The transmitting section integrates a PLL and a bridge driver that is formed by two push-pull drivers driven by two signals 180° phase shifted. The receiving section contains a synchronous demodulator (sampler) and a filtering chain. The chain achieves a band-pass-filtering function defined by two low-frequency zeroes, depending of Cdec and Cdc2 capacitors and a high frequency pole built-in, in the range of 10kHz.



Trace A: C_{DC2}=10nF, trace B: C_{DC2}=6.8nF

Figure 4: EM4095 filtering characteristics

The filtering should be adapted according to the used transponder data-rate (e.g. 2 kbit/s). Refer to chapters 3.7 and 4.8 for more detailed information.

2.3 System performance evaluations

EM will be glad helping you to design your 125 kHz RFID basestation using EM4095 front-end for your custom application. EM provides an Excel -sheet to calculate parameters of an RFID system using the EM4095. The file is available on the EM Microelectronic-Marin SA homepage:

http://www.emmicroelectronic.com

3 Design tips

Reliability of a reader application using the EM4095 transceiver can be optimized following some basic design rules pointed out in this chapter.

3.1 Board design

Pins DVDD and DVSS should be connected to VDD and VSS respectively. Care should be taken that voltage drops due to driver current which is flowing through pins DVDD and DVSS does not provoke voltage drops on VDD and VSS. The DVSS pin and DVDD pin should be blocked by a 100nF capacitor between the two pins as close as possible to the chip. This should prevent the supply spikes caused by the antenna drivers. Blocking of the analog supply pins VSS and VDD next to the chip is also advisable. Blocking capacitors are not included in the EM4095 application schematics.

All capacitors related to pins DC2, AGND and DMOD_IN should be connected to the same VSS line, which should be connected directly to VSS pin of the chip. This VSS line should not be connected to other elements or be a part of "supply line" going to DVSS.

The interconnecting lines to all the sensitive pins (listed above) must be as short as possible. This is also true for the VSS line to the blocking capacitors. The capacitive coupling from all "hot" lines specially the digital output DEMOD_OUT to the sensitive input pins DEMOD_IN, FCAP, CDEC, DC2 and AGND should be avoided.

EM can provide a sample PCB with EM4095, power supply filter caps and caps on DEMOD_IN, FCAP, CDEC, DC2 and AGND already mounted.

A PCB layout can also be found on EM Microelectronic-Marin SA homepage.

http://www.emmicroelectronic.com/

3.2 Power supply stability

Since ANT drivers drive antenna with VDD and VSS power supply level it is clear that all variations and noise in power supply are directly fed to antenna resonant circuit. Any supply variation which will result in variation of antenna high voltage in mV region will result in reduced functionality or even malfunction of the system (transponder signal superimposed on antenna voltage is in the range of tens of mV). Special care has to be taken to filter low frequency noise in range up to 20 kHz since the transponder signal is in this frequency range.

3.3 Analog ground pin AGND

The AGND capacitor can be increased from 220nF up to 1uF. The bigger capacitor value can slightly reduce the receive noise. The AGND voltage is filtered by external capacitor and internal resistor of 2kohms.

3.4 Design of DEMOD_IN capacitive divider

Capacitor divider should be designed in a way that parasitic capacitances (few pF of DMOD_IN pin, parasitics of PCB, …) do not influence divider ratio. Capacitor with value from 1 to 2 nF is proposed for connection from DMOD_IN pin to VSS (C_{DV2}). Capacitor from antenna high voltage point to DMOD_IN (C_{DV1}) pin is then calculated from divider ratio.

Additional capacitance of capacitive divider must be compensated by accordingly smaller resonant capacitor.

3.5 Maximum current on ANT driver outputs

EM4095 is not limiting the current delivered by ANT drivers. Absolute maximum rating on these two outputs is 300 mA. Design of antenna resonant circuit connected to ANT drivers must be done in a way that maximum peak current of 250 mA is never exceeded. If quality of antenna is so high that this current might be exceeded, it has to be reduced by adding series resistor. As already mentioned in EM4095 datasheet [1] antenna driver current also defines the maximum operating temperature. Maximum peak current should be designed in a way that internal junction temperature does not exceed maximum junction temperature at maximum application ambient temperature. Based on maximum current and temperature range a choice of packaging has to be done. Low cost package SOIC 16 has Thermal Convection of 70 °C/W and PSOP has 30 °C/W with a special PCB layout (refer to EM4095 Data Sheet).

3.6 Signal MOD

It is recommended to connect MOD to VSS in read-only applications.

EM4095 has some built in test features, which are switched on when SHD and MOD pins are high. It is thus recommended that MOD pin is kept low while SHD is high.

3.7 Band pass filter tuning

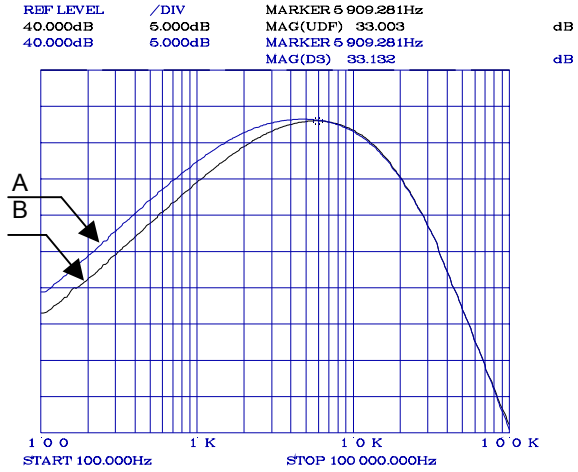
The reception filtering is done in two stages. The first stage zero is defined by external capacitor Cdec and internal resistor (100 kohms). The pole of the first stage is set internally to ~ 25 kHz. The second stage zero is defined by external capacitor Cdc2 and internal resistor. The pole of the second stage is defined internally to 12 kHz.

This means that the reception poles can not be changed and the upper frequencies are limited by two stages filter having -3dB frequencies at 25 kHz and 12 kHz.

The two stage zeroes can be changed (refer to chapter 4.8).

The default settings should be at about Cdec = 100nF and Cdc2 = 10nF. This combination is more than sufficient to fulfill the sensitivity specification and to enable reliable operation.

Increasing the Cdc2 capacitor (max. 22 nF) will in real application increase the receive sensitivity, specially if the Q of the transponder is high, which causes non-rectangular (sloped) receive input signal.

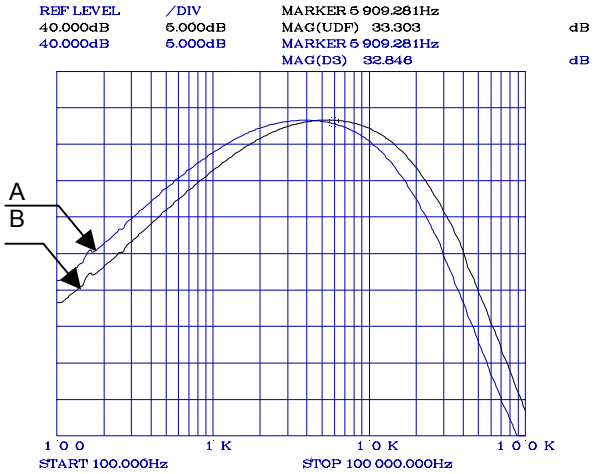


Trace A: C_{DC2}=10nF, trace B: C_{DC2}=6.8nF

Figure 5: Filtering characteristic as function of filter capactior Cdc2

Increasing the Cdc2 capacitor will increase the receive bandwidth what in consequence increases the receive gain for sloped signals.

The advisable range for Cdc2 is from 6.8 nF to 22nF and Cdec from 33 nF to 220 nF. A higher capacitor value can increase the start-up time.



C_{DC2}=10nF: trace A: -30°C, trace B: 90°C

Figure 6: Filtering characteristic as function of temperature

4 Calculating an example

The following example presents the EM4095 front-end using on-off-keying (OOK) communication protocol from the reader to transponder (uplink). Helpful equations can be found in [2]. They can be used for principal design, but the calculations have to be verified by measurement. Eventually the results have to be adjusted to compensate possible parasitics and second order effects.

A reader system with a high Q antenna will be specified. The system will operate at

f_0 = 125 kHz

and ambient temperature range

-40 to 85°C.

4.1 Reader antenna properties

To design a low cost read/write (R/W) basestation using OOK communication protocol for the uplink communication, the configuration according to the chapter "Typical Operating Configuration" - fig. 2 - has been chosen [1].

4.1.1 Reader antenna inductivity

The antenna inductivity is usually chosen from within the range from 300 uH to 800 uH. In this example the following inductivity and quality factor have been selected

L_A = 725 uH ± 1%
Q_A = 40.

4.1.2 Reader antenna resistance

The ohmic antenna resistance can be found by applying the formula

$$R_{ANT} = \frac{2\pi f_0 L_A}{Q_A}$$

R_{ANT} = 14.23 Ω

Specified by [1], the antenna driver resistance and the power supply voltage of

R_{AD} = 3 Ω
VDD - VSS = 5V

will be used in following calculations.

4.1.3 Resonant capacitor

System will operate at 125 kHz. The resonant capacitor C_{RES} is calculated by

$$C_{RES} = \frac{1}{(2\pi f_0)^2 L_A}$$

C_{RES} = 2.24 nF

Remark: Until that point of the calculation, C_{dv1} and C_{dv2} effect is neglected, as they are not yet calculated. (see 4.4 for real resonant frequency value).

4.1.4 Reader antenna current and voltage

By the given antenna driven in the bridge-driver configuration [1] and applying the equations

$$I_{ANT(peak)} = \frac{4}{\pi} \frac{V_{dd} - V_{ss}}{R_{ANT} + R_{SER} + 2R_{AD}}$$

and

$$V_{ANT(peak)} = \frac{I_{ANT(peak)}}{2\pi . f_o . C_{RES}}$$

the current and the voltage at the reader antenna are (Rser=0):

$I_{ANT(peak)}$ = 315 mA
$V_{ANT(peak)}$ = 182 V

To suite the maximum specifications at DEMOD_IN [1], the antenna voltage would have to be divided by nearly a factor of

d_C = 100.

Decimating the antenna voltage ensures a proper demodulation of the received transponder data signal.

Applying a serial resistor RSER to the resonance circuit can reduce the division factor d_c.

4.1.5 Reader antenna quality factor

Practical antenna circuit Q factors, in case full receiver chain is used, can be found between 10 and 15. Introducing a serial resistor R_{SER}, will limit the high voltage by reducing the overall quality factor, without reducing reading distance.

To conclude, the resonance circuit quality factor Q can be reduced by adding a serial resistor R_{SER}.

Reduced Q also improves recovery time after modulation, which is especially important for transponders with data rates at 32 and 40 periods per bit. Furthermore a lower antenna current will limit the junction temperature of the chip.

The following calculations are based on a serial resistor of

R_{SER} = 33 Ω

which has been calculated iteratively by using the equations from chapter 4.1.4.

The resulting antenna current and voltage in resonance are more suitable

$I_{ANT(peak)}$= 119.59 mA,
$V_{ANT(peak)}$ = 69.22 V.

4.2 Capacitor divider

The input signal at DEMOD_IN has to be limited by a division factor d_C, to meet the EM4095 common mode range specifications [1].

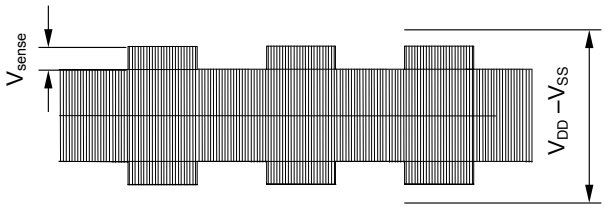


Figure 7: Decimated antenna signal at DEMOD_IN

At this point a measurement was performed using elements described above. The resulting amplitude at the antenna was

$V_{ANT(pp)}$ = 140 Vpp

which is close to the calculated value.

Regarding the common mode range at DEMOD_IN, the capacitor divider can be calculated taking the measured peak-peak voltage on antenna into account.

$$d_C < \frac{V_{Ant(pp)}}{V_{DEMOD\_IN\_\max}}$$

At $V_{DEMOD\_IN\_PP}$ = 4V_{PP} a division factor of

d_C = 35

seems to be good choice, while such a division ratio can be done using standard capacitors. Recommended capacitor value of C_{DV2} is in the range of 1 nF to 2 nF.

The following capacitors have been chosen:

C_{RES} = 2.2 nF
C_{DV1} = 47 pF
C_{DV2} = 1.5 nF

A tolerance class of ± 2 % is acceptable for the capacitors above. Together with a tolerance of ± 1 % of L_A, an overall tolerance of ± 1.5 % on f_0 can be specified.

4.3 Real Resonant frequency:

A fine calculation of the resonant frequency should take into account the C_{dv1} and C_{dv2} capcitor as indicated in this formula:

$$C_o = C_{RES} + \frac{C_{DV1}.C_{DV2}}{C_{DV1} + C_{DV2}}$$

This equivalent resonant capacitor value can be used to recalculate the resonant frequency f_0:

$$f_0 = \frac{1}{2\pi\sqrt{L_A.C_0}}$$

4.4 Sensitivity to reader antenna signal

Using parameter V_{sense} we can calculate sensitivity for transponder signal on antenna high voltage point.

$$V_{DMOD\_IN(pp)} = V_{ANT(pp)} \frac{C_{DV1}}{C_{DV1} + C_{DV2}}$$

Having a division factor d_C = 33, as in the example and respecting the minimum sensitivity of 0.85 mV_{PP} at DEMOD_IN [1] a minimum modulation of

V_{Sense_ant} = 28.05 mV_{PP}

on the reader antenna can be detected by the EM4095.

4.5 Power dissipation

The power dissipation of the reader can be calculated by starting with the equation

$$I_{ANT(pp)} = V_{ANT(pp)} \cdot 2\pi \cdot f_0 \cdot C_0$$

$I_{ANT(peak)}$ = 114 mA.

Once the AC antenna current is found, I_{RMS} can be calculated using equation

$$I_{RMS} = \frac{I_{ANT(peak)}}{\sqrt{2}}$$

I_{RMS} = 81 mA.

To calculate the power dissipation, further parameters are of concern. Firstly, the maximum value of ANT driver resistor [1]

R_{AD} = 9 Ω

and secondly, the maximum value of supply current, provided by the EM4095 [1]

I_{DDon} = 10 mA.

Finally, the total power dissipation is calculated by

$$P = 2 \cdot I_{RMS}^{\ 2} \cdot R_{AD} + I_{DDon}\left(V_{DD} - V_{SS}\right)$$

P = 167 mW.

4.6 Temperature

Worst case calculations on temperature increase on a low cost SOIC 16 case with R_{Th}=70 °C/W [1] and P = 167 mW are performed using

$$\Delta T = P \cdot R_{Th}$$

ΔT = 11.7 K.

The maximum junction temperature T_j is specified to remain below 100°C [1]. The designer has to ensure proper functionality of the design.

4.7 Signal damping

Since antenna voltage V_{Ant} is approx. 140 V_{PP} this corresponds to:

$$L_V = 20 \cdot \log \frac{V_{Ant}}{V_{Sense\_ant}}$$

$$L_V = 20 \cdot \log \frac{140 V_{PP}}{28{,}05.10^{-3} V_{PP}} = 74 dB$$

4.8 Band-pass filter tuning

As already mentioned in chapter 3.7, default settings for Cdec and Cdc2 can be used.

Cdec = 100nF,
Cdc2 = 10nF.

The zero-transition frequency is given by

$$f_Z = \frac{1}{2 \cdot \pi \cdot R \cdot C}$$

and for the first zero frequency = 16 Hz @ Cdec = 100nF. For the second zero frequency = 1.5 kHz @ Cdc2 = 10nF.

Adapting these coefficients can optimize the receiving sensitivity.

For more detailed information refer to [2] and [3].

5 Interfacing a read-only transponder: e.g. EM4100

Basic concepts connecting the EM4095 to a microcontroller are pointed out in this chapter. A typical EM4095 setup to communicate with a read-only transponder (e.g. EM4100) is shown.

5.1 Microcontroller interface

The microcontroller is connected to the EM4095 through a slim three-wire-interface using the signals SHD, RDY/CLK and DEMOD_OUT.

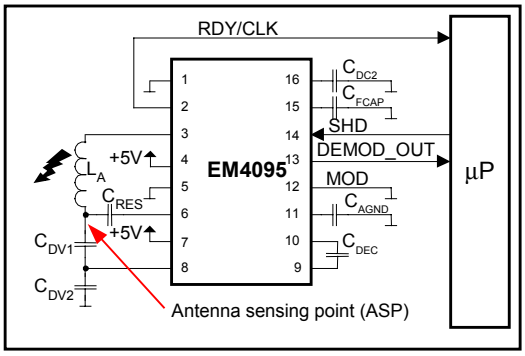


Figure 8: Typical read-only setup

5.1.1 Sleep mode (SHD)

The EM4095 can be put in sleep mode by applying V_{DD} on the pin SHD. SHD is high active. The consumption in sleep mode is specified to only 1µA [1].

SHD = 1	sleep mode
SHD = 0	operation mode

5.1.2 Modulation (MOD)

By applying V_{DD} on MOD, a modulation of 100 % is performed.

MOD = 1	100% of modulation
MOD = 0	no modulation

The antenna current will be:

$$I_{ANT(peak)} = \frac{4}{\pi} \frac{V_{dd} - V_{ss}}{R_{ANT} + R_{SER} + 2R_{AD}}$$

See chapter 5.2 on how to control the electromagnetic field with the microcontroller.

5.1.3 Ready and clock signal (RDY/CLK)

The RDY/CLK signal offers multiple functionality to observe either the EM4095 ready to run (RDY) or by sorting a synchronous signal (CLK) to the data on DEMOD_OUT.

The RDY signal is also available, when the antenna drivers are in off-state, which is forced by setting MOD = 1.

5.2 Command transmission (uplink)

Since it is sufficient to generate a constant electromagnetic field to communicate with read-only transponders, the MOD pin is not connected to the microcontroller but is therefore fixed to VSS.

5.3 Signal reception on DEMOD_IN

By following the calculation example (previous chapter) a decimated antenna signal should show a similar signal on your oscilloscope. The upper trace shows the DEMOD_OUT, while the lowest trace shows the transponder antenna signal.

Traces:

Ch1 DEMOD_OUT
Ch2 Transponder antenna signal (measured with a spy coil)

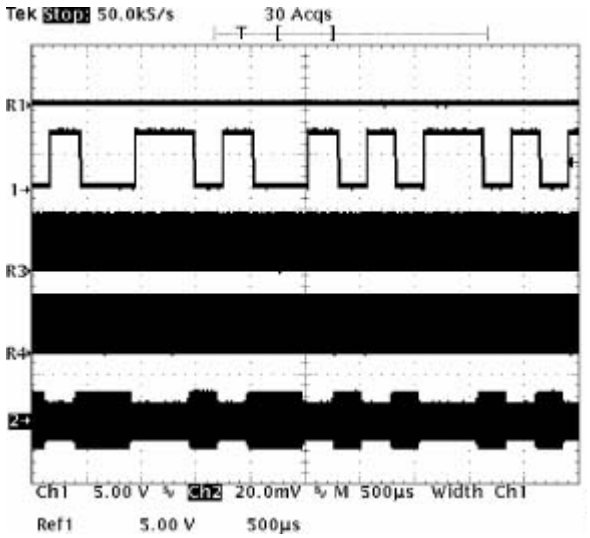


Figure 9: Demodulated transponder signal and transponder antenna signal

6 Interfacing a read/write transponder: e.g. EM4069

A typical EM4095 setup to communicate with a read-write transponder (e.g. EM4069) is shown in this chapter.

6.1 Microcontroller interface

The microcontroller is connected to the EM4095 through a slim interface using the signals SHD, RDY/CLK, MOD and DEMOD_OUT. The serial resistance R_{AM} allows the specification of an individual modulation index m_{MOD}. This features offers to communicate e.g. with the R/W transponder P4069.

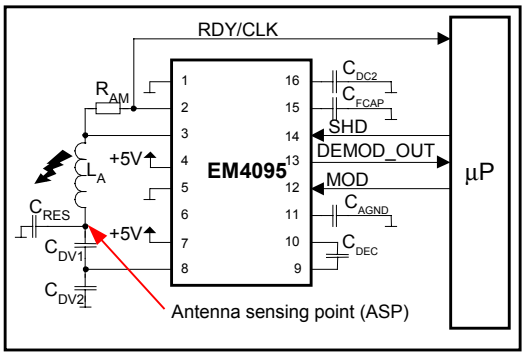


Figure 10: Typical R/W setup with specific modulation index

6.1.1 Sleep mode (SHD)

The EM4095 can be put in sleep mode by applying V_{DD} on the pin SHD. SHD is high active. The consumption in sleep mode is specified to only 1µA [1].

SHD = 1	sleep mode
SHD = 0	operation mode

6.1.2 Modulation (MOD)

By applying V_{DD} on MOD, a modulation index is specified, by adding resistor R_{AM}. At R_{AM} = 0, a modulation of 100% will be achieved.

MOD = 1	modulation according to the modulation index m_{MOD}
MOD = 0	no modulation

The antenna current is specified by:

$$I_{ANT} = \frac{2}{\pi} \frac{V_{dd} - V_{ss}}{R_{ANT} + R_{AM} + R_{SER} + 2R_{AD}}$$

For applications using read-only transponders, the MOD pin can be connected to V_{SS} by default.

6.1.3 Ready and clock signal (RDY/CLK)

The RDY/CLK signal offers multiple functionality to observe either the EM4095 ready to run (RDY) or by sorting a synchronous signal (CLK) to the data on DEMOD_OUT.

The RDY signal is also available, when the antenna drivers are in off-state, which is forced by setting MOD = 1.

6.2 Command transmission (uplink)

To generate a variable electromagnetic field, the MOD pin is connected to the microcontroller.

Trace:

Ch1	reader antenna signal
Ch3	triggering signal
Ch2	MOD signal

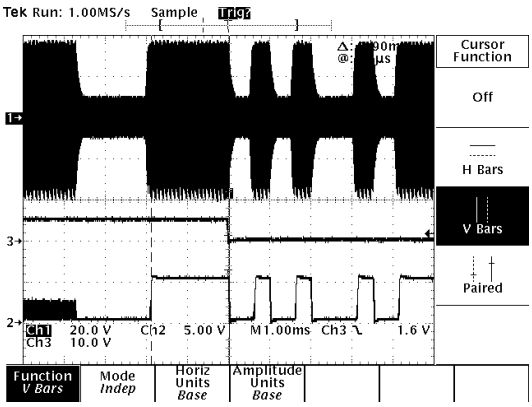


Figure 11: Reader antenna signal on uplink

6.3 Signal reception on DEMOD_IN

By following the calculation example (previous chapter) a decimated antenna signal should show a similar signal on your oscilloscope. The upper trace shows the DEMOD_IN, while the lowest trace shows the demodulated transponder signal.

Traces:

Ch1 DEMOD_OUT
Ch2 antenna signal (measured with a spy coil)

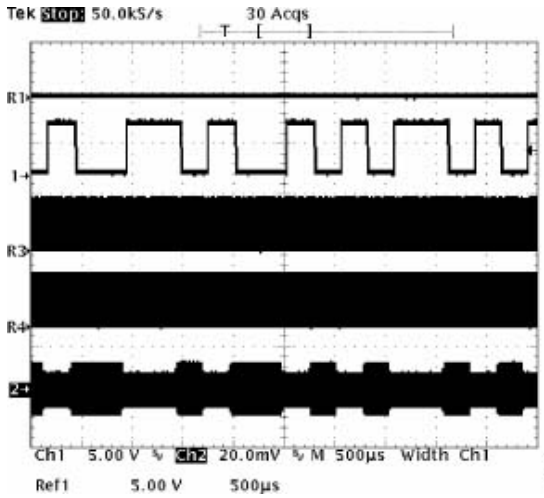


Figure 12: Antenna signal and demodulated transponder data

7 Interfacing a read/write transponder: e.g. EM4150

A typical EM4095 setup to communicate with a read-write transponder (e.g. EM4150) is shown in this chapter.

7.1 Microcontroller interfache

The microcontroller is connected to the EM4095 through a slim interface using the signals SHD, RDY/CLK, MOD and DEMOD_OUT.

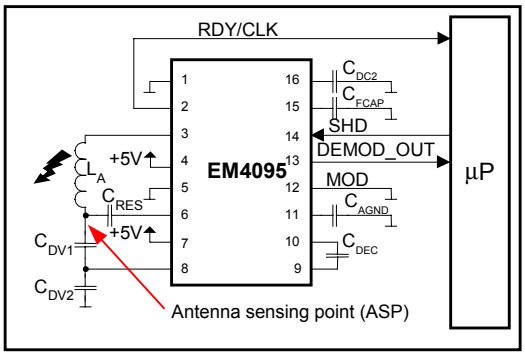


Figure 13: Typical R/W setup using brigde-driver configuration

7.1.1 Sleep mode (SHD)

The EM4095 can be put in sleep mode by applying V_{DD} on the pin SHD. SHD is high active. The consumption in sleep mode is specified to only 1µA [1].

SHD = 1	sleep mode
SHD = 0	operation mode

7.1.2 Modulation (MOD)

By applying V_{DD} on MOD, a modulation of 100 % is performed.

MOD = 1	100% of modulation
MOD = 0	no modulation

Since fig. 10 shows the bridge-driver configuration [1], the antenna current is specified by:

$$I_{ANT(peak)} = \frac{4}{\pi} \frac{V_{dd} - V_{ss}}{R_{ANT} + R_{SER} + 2R_{AD}}$$

7.1.3 Ready and clock signal (RDY/CLK)

The RDY/CLK signal offers multiple functionality to observe either the EM4095 ready to run (RDY) or by sorting a synchronous signal (CLK) to the data on DEMOD_OUT.

The RDY signal is also available, when the antenna drivers are in off-state, which is forced by setting MOD = 1.

7.2 Command transmission (uplink)

To generate a variable electromagnetic field, the MOD pin is connected to the microcontroller.

Traces:

R1	MOD
R2	DEMOD_OUT
R3	ANT1
R4	RDY/CLK
Ch2	transponder antenna signal (measured with a spy coil)

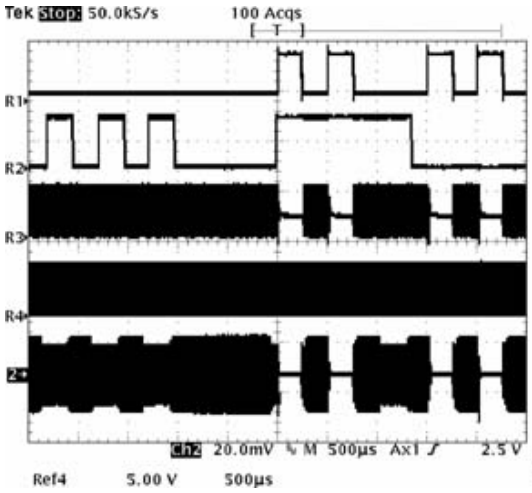


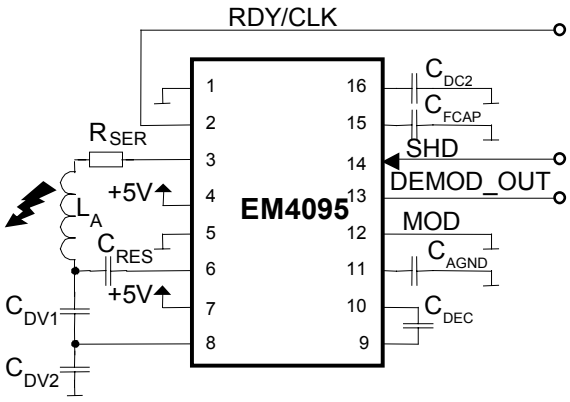
Figure 14: Transmission and reception signal on the EM4095

8 Schematic and PCB

The EM4095 demonstration board provided by EM Microelectronic-Marin SA offers plug-and-play capability for designers. All signals for control and reception are available on a connector. Control signals can either be generated by a pattern generator or by connecting the designer's favourite microcontroller. As a special feature, the reader antenna is integrated on the PCB. The reading range is about 11 cm.

The schematic and PCB files are also available from http://www.emmicroelectronic.com.

8.1 Schematic of the EM4095 demo board



Components:

C_{DC2}	10 nF
C_{FCAP}	10 nF
C_{AGND}	100 nF
C_{DEC}	100 nF
C_{RES}	10 nF + 1 nF
C_{DV1}	100 pF + 47 pF
C_{DV2}	1 nF
R_{SER}	15 Ω
L_A	120 µH
V_{DD}, DV_{DD}	5V
I_{DC}	ca. 90 mA
C_1 (DV_{DD} supply)	100 nF
C_2 (DV_{DD} supply)	3.3 µF
C_4 (V_{DD} supply)	100 nF

Figure 15: EM4095 basic reader schematic

8.2 Printed Circuit Board (PCB) of the EM4095 demo board

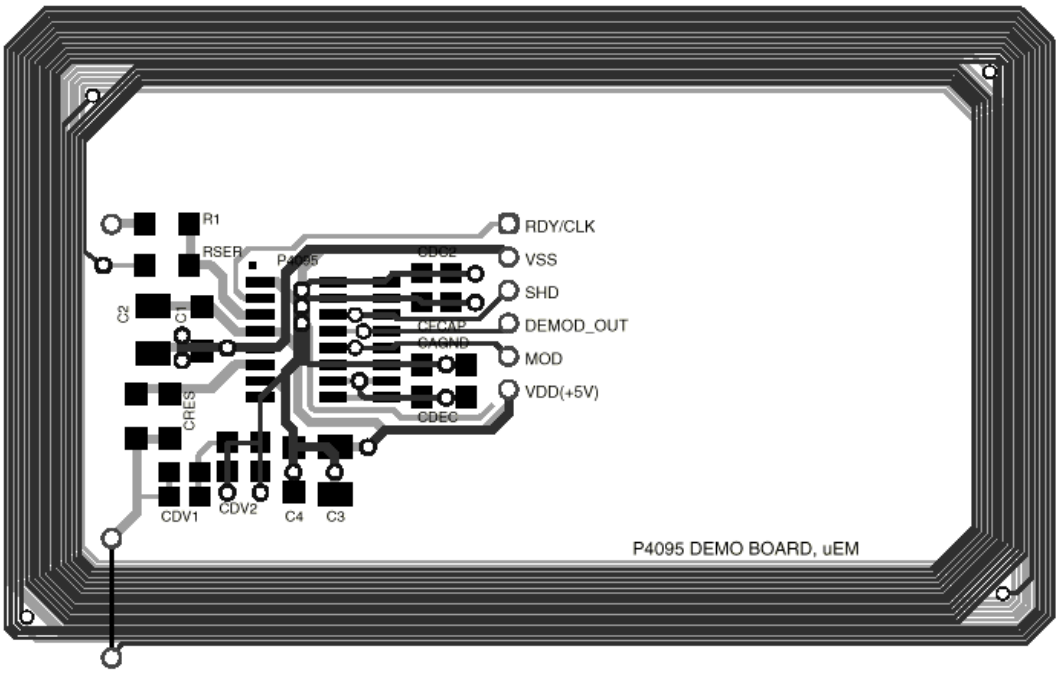


Figure 16: EM4095 demo board with integrated antenna

A. Notes